**DAILY ASSESSMENT FORMAT**

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| **Course:** | **VLSI design** | **USN:** | **4al16ec074** |
| **Topic:** | **CMOS Inverter Basics** | **Semester & Section:** | **8-B** |
| **Github Repository:** | **shreya-test** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report**  **The Static CMOS Inverter**  Its operation is readily understood with the aid of the simple switch model of the MOS transistor, : the transistor is nothing more than a switch with an infinite offresistance (for |VGS| < |VT |), and a finite on-resistance (for |VGS| > |VT |). This leads to thefollowing interpretation of the inverter. When Vin is high and equal to VDD, the NMOS transistor is on, while the PMOS is off. This yields the equivalent circuit of Figure a. A direct path exists between Vout and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), NMOS and PMOS transistors are off and on, respectively. The equivalent circuit of Figure b shows that a path exists between VDD and Vout, yielding a high output voltage. The gate clearly functions as an inverter.  A number of other important properties of static CMOS can be derived from this switchlevel view: • The high and low output levels equal VDD and GND, respectively; in other words, the voltage swing is equal to the supply voltage. This results in high noise margins. • The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. Gates with this property are called ratioless. This is in contrast with ratioed logic, where logic levels are determined by the relative dimensions of the composing transistors. • In steady state, there always exists a path with finite resistance between the output and either VDD or GND. A well-designed CMOS inverter, therefore, has a low output impedance, which makes it less sensitive to noise and disturbances. Typical values of the output resistance are in kW range. • The input resistance of the CMOS inverter is extremely high, as the gate of an MOS transistor is a virtually perfect insulator and draws no dc input current.  Since the input node of the inverter only connects to transistor gates, the steady-state input current is nearly zero. A single inverter can theoretically drive an infinite number of gates (or have an infinite fan-out) and still be functionally operational; however, increasing the fan-out also increases the propagation delay, as will become clear below. So, although fan-out does not have any effect on the steady-state behavior, it degrades the transient response.    The nature and the form of the voltage-transfer characteristic (VTC) can be graphically deduced by superimposing the current characteristics of the NMOS and the PMOS devices. Such a graphical construction is traditionally called a load-line plot. It requires that the I-V curves of the NMOS and PMOS devices are transformed onto a common coordinate set. We have selected the input voltage Vin, the output voltage Vout and the NMOS drain current IDN as the variables of choice. The PMOS I-V relations can be translated into this variable space by the following relations (the subscripts n and p denote the NMOS and PMOS devices, respectively): (5.1) The load-line curves of the PMOS device are obtained by a mirroring around the xaxis and a horizontal shift over VDD. This procedure is outlined in Figure 5.3, where the subsequent steps to adjust the original PMOS I-V curves to the common coordinate set Vin, Vout and IDn are illustrated. IDSp I = – DSnVGSn Vin VGSp= ; = Vin – VDD VDSnVoutVDSp = ; = Vout – VDD |